

**IN THE CLAIMS:**

Claims 1, 2, 5, and 7 have been amended herein. Please cancel claim 6 without prejudice or disclaimer. Please note that all claims currently pending and under consideration in the above-referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (Currently amended) A method of forming an interconnect in an oxide isolation region immediately adjacent to an active area of an integrated circuit, comprising:

providing a substrate assembly comprising a silicon substrate having at least one vertically extending segment, wherein the at least one vertically extending segment is doped to form an active area;

masking the active area with a nitride layer, wherein an edge of the nitride layer is aligned with a lateral edge of the active area that abuts ~~the~~an oxide isolation region;

forming a trench in the silicon substrate and filling the trench with a dielectric material to form the oxide isolation region;

exposing the oxide isolation region and a portion of the nitride layer to an etch process that etches the oxide isolation region faster than the nitride layer such that a portion of the oxide isolation region is removed to form a downwardly extending opening in the oxide isolation region that exposes a portion of the lateral edge of the active area; and

at least partially filling the downwardly extending opening with a polysilicon material such that the polysilicon material contacts the active area to form the interconnect.

2. (Currently amended) A method of forming an interconnect in a dielectric isolation region immediately adjacent to an active silicon area of an integrated circuit, wherein the dielectric isolation region and the active silicon area share a common vertical interface, the method comprising:

providing a substrate assembly comprising a silicon substrate having at least one vertically extending segment, wherein the at least one vertically extending segment is doped to form an active silicon area;

masking a region of a top surface of the active silicon area with a nitride layer, wherein a lateral edge of the nitride layer is aligned with a lateral edge of the active silicon area along ~~the~~ a common vertical interface;

forming a trench in the silicon substrate and filling the trench with a dielectric material to form a dielectric isolation region;

exposing a selected area of the dielectric isolation region and a portion of the nitride layer to an etch environment that etches the dielectric isolation region faster than the nitride layer such that a portion of the dielectric isolation region is removed to form a downwardly extending opening in the dielectric isolation region that exposes a portion of the ~~active area~~ common vertical interface; and

filling the downwardly extending opening with a polysilicon material such that the polysilicon material contacts the active area to form ~~the~~ an interconnect.

3. (Original) The method of claim 2, wherein the dielectric isolation region comprises borophosphosilicate glass.

4. (Original) The method of claim 2, wherein the nitride layer is vertically separated from the active area by a layer of oxide.

5. (Currently amended) A method of forming a structure on a substrate assembly, the method comprising:

providing an integrated circuit substrate assembly comprising a silicon substrate having at least one vertically extending segment, wherein the at least one vertically extending segment is doped to form an active area;

providing a vertical edge of ~~an~~ the active area within ~~an~~ the integrated circuit substrate assembly;

forming a region of a first dielectric material immediately adjacent to and in contact with the vertical edge of the active area;

forming a nitride layer above the active area and in alignment with the vertical edge;

forming a trench in the silicon substrate and filling the trench with a second dielectric material;

etching a hole into the region of the first dielectric material at the vertical edge, wherein the hole is etched with an etching process that selectively etches the region of the first dielectric material at a faster rate than the etching process etches the nitride layer such that the active area is not etched; and

filling at least a portion of the hole with a volume of electrically conductive material within the region of the first dielectric material, the volume of electrically conductive material being situated in contact with the vertical edge, the region of the first dielectric material making a planar interface in contact with the vertical edge.

Claim 6 (Canceled)

7. (Currently amended) A method of forming an interconnect structure on an integrated circuit, comprising:

providing a substrate assembly comprising a silicon substrate having at least one vertically extending segment, wherein the at least one vertically extending segment is doped to form an active area;

forming a silicon nitride layer above a the silicon substrate of the integrated circuit;

etching a trench through the silicon nitride layer and into the silicon substrate to expose a vertical edge within the silicon substrate that is orthogonal to a top plane of the silicon substrate;

filling the trench with a dielectric material to form an isolation region;

etching a hole into the isolation region at the vertical edge with an anisotropic etch to selectively etch the dielectric material at a faster rate than the anisotropic etch etches the silicon nitride layer;

forming a polysilicon plug within at least a portion of the hole such that the polysilicon plug is situated to the side of, in contact with, and immediately adjacent to the vertical edge and such that the polysilicon plug forms a planar and vertical interface with the silicon substrate; and

implanting dopants into the silicon substrate to form an active region adjacent the vertical interface.